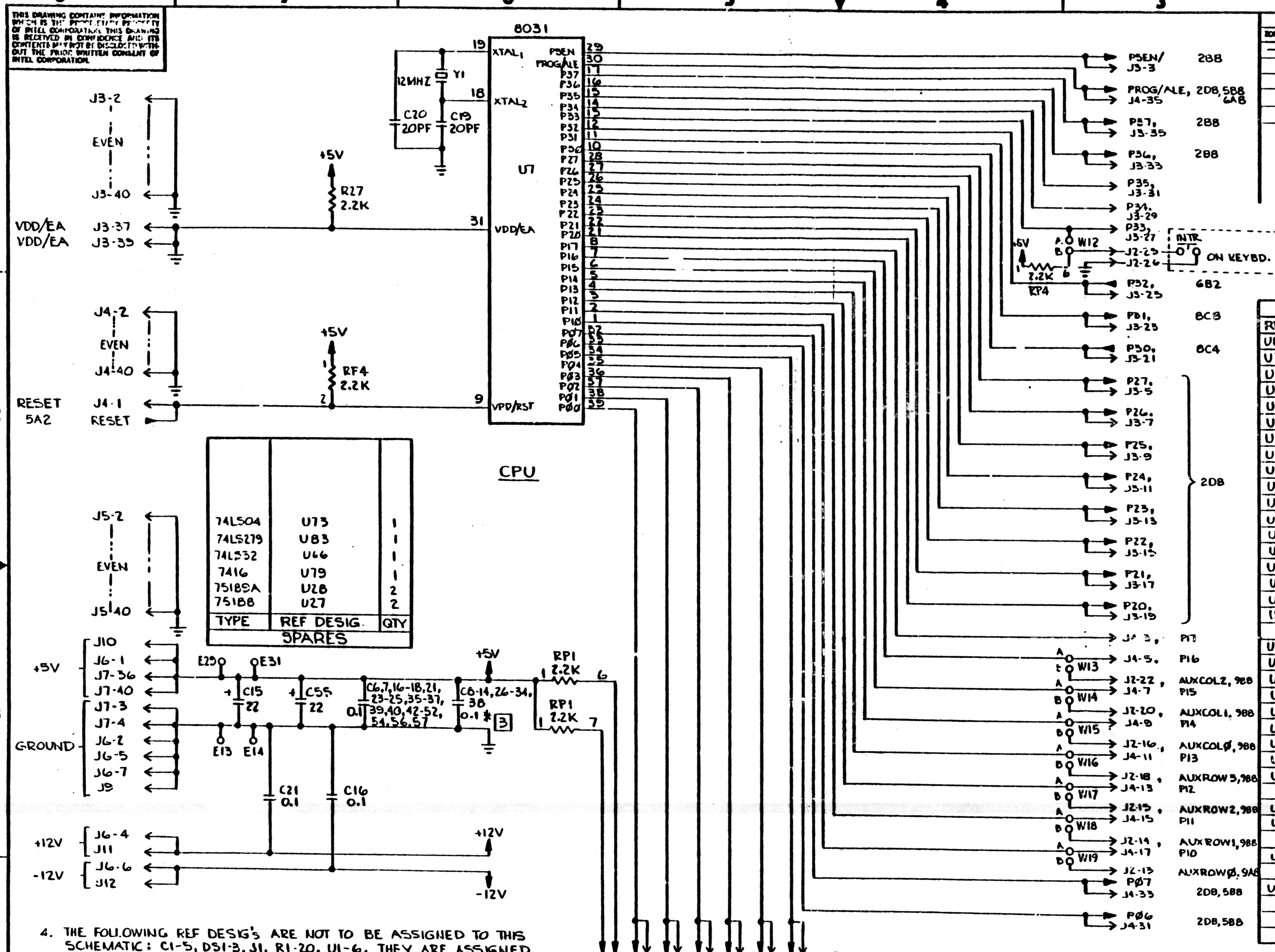
DWG NO.	SH	REV
162072	1	A

REVISIONS

ZONE	REV	DESCRIPTION	DFT	CHK	DATE	APPROVED
—	A	ECO 14-0480				



TYPE	REF DESIG.	QTY
74LS04	U73	1
74LS279	U83	1
74LS32	U66	1
7416	U79	1
75189A	U28	2
75188	U27	2

SPARES

POWER AND GROUND LOCATOR CHART

REFERENCE DESIGNATOR	TYPE	GND	+5V	+12V	-12V
U84	74LS02	7	14		
U73	74LS04	7	14		
U78,79	7416	7	14		
U52	74LS08	7	14		
U75	74LS10	7	14		
U76	74LS11	7	14		
U71	74LS14	7	14		
U66,72,85	74LS32	7	14		
U39,53	74LS85	8	16		
U26,51	74LS138	8	16		
U67	74LS139	8	16		
U40,55,74,77	74LS161	8	16		
U80,81,82	74LS164	7	14		
U38	74S138	8	16		
U42,86	74LS244	10	20		
U83	74LS279	8	16		
U69,70	74LS367	8	16		
U8,17	74LS373	10	20		
U9-16,18-25,30-37,43-50	2114AL	9	18		
U61,62	2141-5	9	18		
U59,60	2732A	12	24		
U7	8031	20	40		
U41	8041A	20	40		
U64	8155-2	20	40		
U54	8243	12	24		
U29	8251A	4	26		
U65	8304	10	20		
U27	75188	7		14	1
U28	75189A	7	14		
U87	LM324	11	4		
U63	3622A-2	8	16		

4. THE FOLLOWING REF DESIG'S ARE NOT TO BE ASSIGNED TO THIS SCHEMATIC: C1-5, DS1-3, J1, R1-20, U1-6. THEY ARE ASSIGNED TO THE DISPLAY BD-SCHEMATIC NO. 162075.

[3] DEVICES INDICATED WITH AN ASTERISK (*) ARE NOT SHIPPED WITH MINIMUM CONFIGURATION KIT.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

1. ALL RESISTANCE VALUES ARE IN OHMS.

NOTES: UNLESS OTHERWISE SPECIFIED

LAST USED	NOT USED
DS4, C62	DS1-3, C1-C5
CR5	
E55	
J12	J1
R48	R1-R20, R44
RF4	
U87	U1-U6
W55	
Y2	

REFERENCE DESIG.

USED ON ASSY NR 162073

NEXT ASSY: SDK 51

UNLESS OTHERWISE SPECIFIED:
1. DIMENSIONS ARE IN INCHES.
2. BREAK ALL SHARP EDGES.
3. DO NOT SCALE DRAWING.
4. TOLERANCES: ANGLES ± 2°, .XX ± .030, .XXX ± .010
SURFACE FINISH

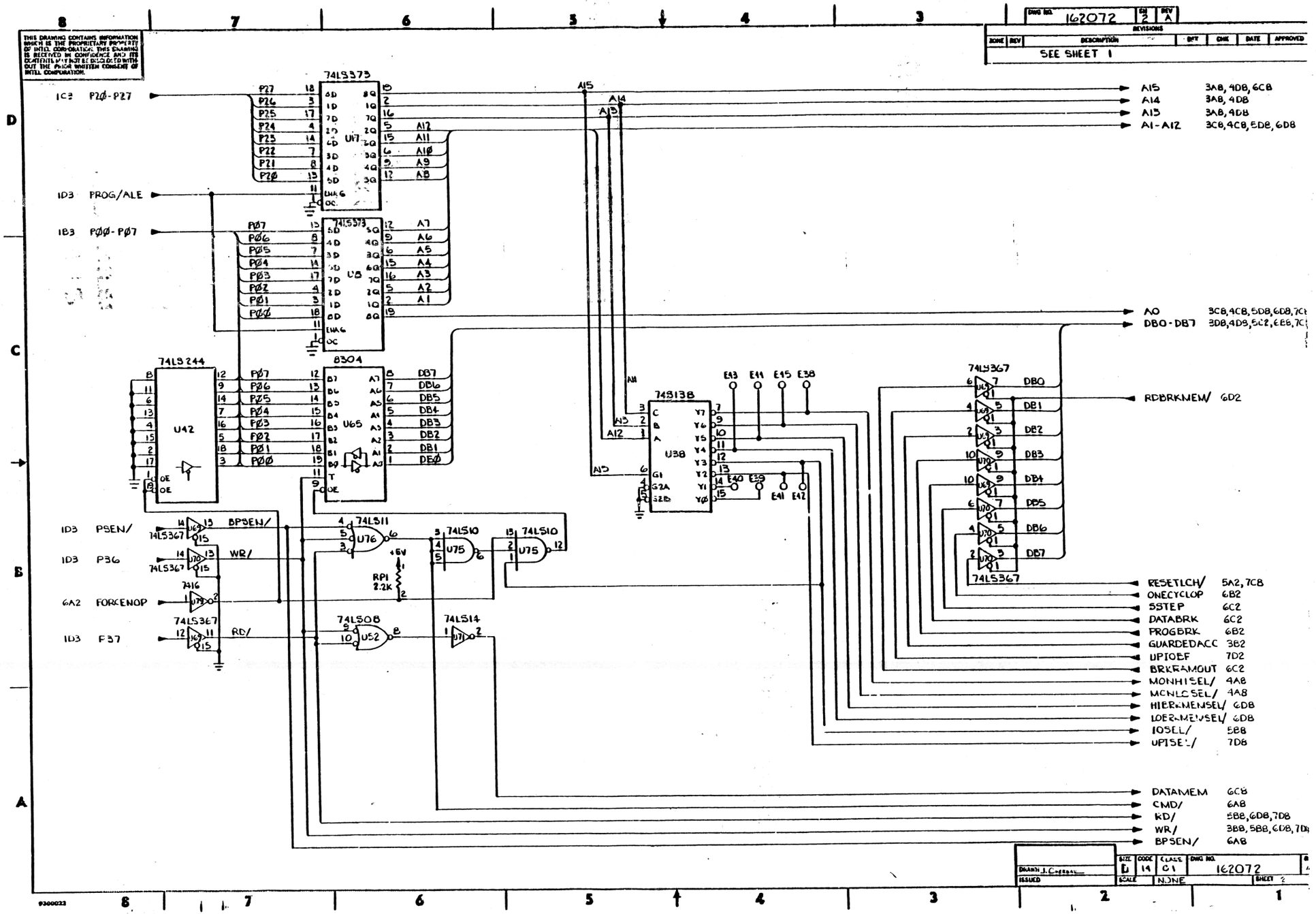
DRN BY J. CHERBAK 3-4-80
CHK BY
APVD D. Olson

intel 3065 BOWERS AVE. SANTA CLARA CALIF. 95051

TITLE: SCHEMATIC, CPU BOARD SDK-51

SIZE	CODE	CLASS	DWG NO.	REV
D	14	01	162072	A

SCALE NONE SHEET 1 OF 9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DWG NO. 162072
REVISIONS
ZONE REV DESCRIPTION DEV CHK DATE APPROVED
SEE SHEET 1
74LS373
U67
74LS373
U8
8304
U65
74LS244
U42
74LS138
U38
74LS367
74LS11
U76
74LS10
U75
74LS08
U52
74LS14
U77
7416
RP1 2.2K
+5V
IC3 P20-P27
ID3 PROG/ALE
IB3 P00-P07
ID3 PSEN/
ID3 P36
6A2 FORCENOP
ID3 P37
BPSEN/
WR/
RD/
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
E43 E41 E45 E38
E40 E39 E41 E42
A15 3A8, 4D8, 6C8
A14 3A8, 4D8
A13 3A8, 4D8
A1-A12 3C8, 4C8, 5D8, 6D8
A0 3C8, 4C8, 5D8, 6D8, 7C
DB0-DB7 3D8, 4D8, 5C2, 6E6, 7C
RDBRKMEM/ 6D2
RESETLCH/ 5A2, 7C8
ONECYCLOP 6B2
SSTEP 6C2
DATABRK 6C2
PROGBRK 6B2
GUARDEDACC 3B2
UPIOEF 7D2
BRKRAMOUT 6C2
MONHISEL/ 4A8
MONLOSEL/ 4A8
HIERMEMSEL/ 6D8
LOERMEMSEL/ 6D8
IOSEL/ 5B8
UPISEL/ 7D8
DATAMEM 6C8
CMD/ 6A8
RD/ 5B8, 6D8, 7D8
WR/ 3B8, 5B8, 6D8, 7D
BPSEN/ 6A8
DRAWN J.C.HERRAL
ISSUED
SIZE D
CODE 14
CLASS C1
DWG NO. 162072
SCALE NONE
SHEET 2
9300023

DWG NO. 162072 SH 5 REV A

REVISIONS

ZONE	REV	DESCRIPTION	DFT	CHK	DATE	APPROVED
		SEE SHEET 1				

2C2 DBØ-DB7

4C2 MEMØSEL/

1A6 TTLH11

2C2 AØ

2D2 A1-A12

2A8 WR/

2D2 A13

2D2 A14

2D2 A15

7D2 TOPØ-TOP6

7C2 CLRBRK/

74LS138 U26 — AØ, A11, A12; G2A, G2D, G1; Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0

U9 U10 U11 U12 U13 U14 U15 U16 — 2114A-5 TYP 16 PLACES — CS, A1–A9, I/O1–I/O4 → DBØ DB1 DB2 DB3

U18 U19 U20 U21 U22 U23 U24 U25 — 2114A-5 TYP 16 PLACES — CS, A1–A9, I/O1–I/O4 → DB4 DB5 DB6 DB7

WE

MEMORY ZERO

74LS85 U39 — A12; TOP4 TOP5 TOP6; A>B A=B A<B

74LS85 U53 — A8 A9 A10 A11; TOPØ TOP1 TOP2 TOP3; A<B A=B A>B

TOP CIRCUIT

74LS32 U66 — RAMWR/ 4B8

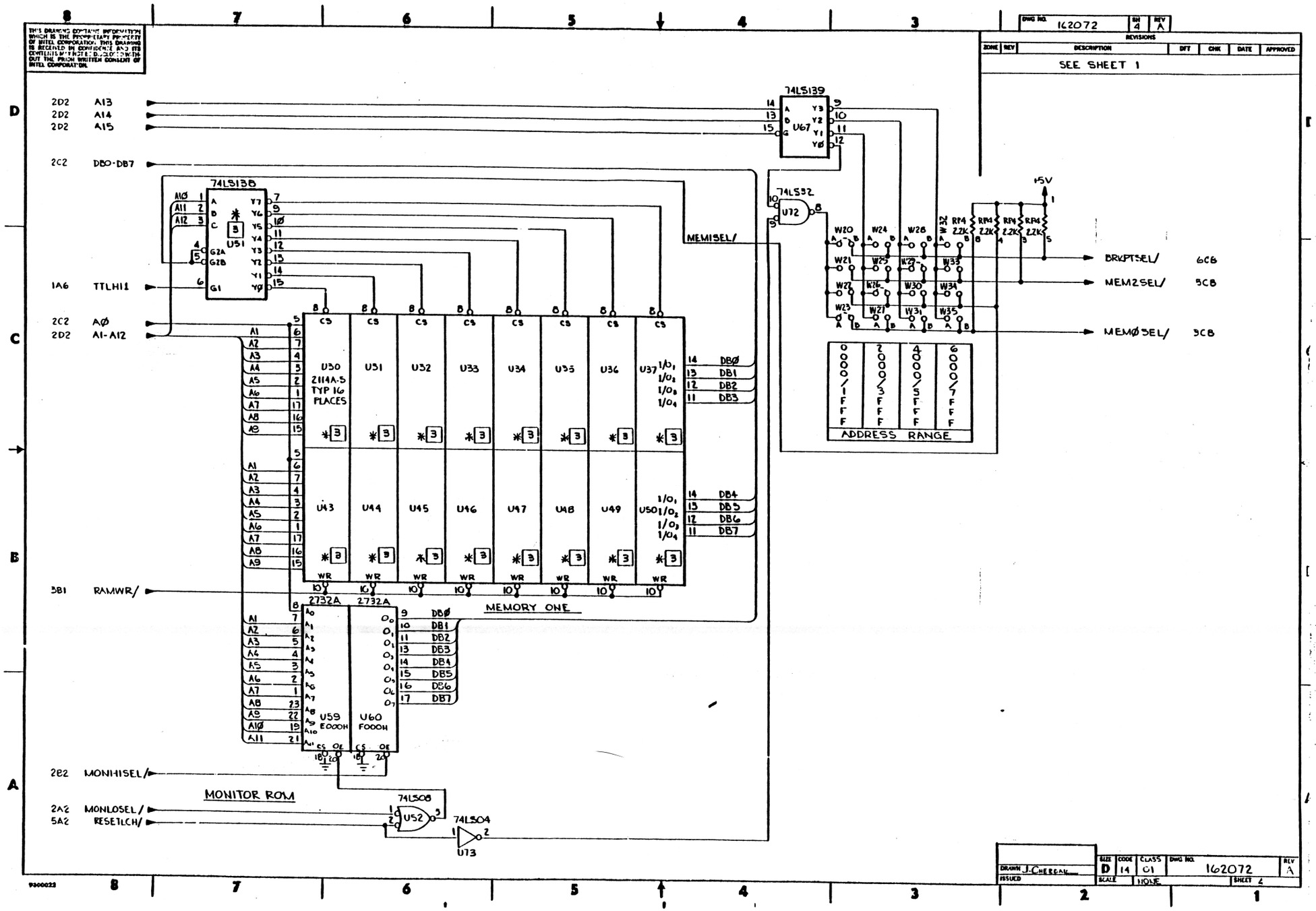
74LS04 U73

74LS32 U72

74LS279 U83 — GUARDEDACC 2B2,6D8

DRAWN J.CHEEBA	SIZE D	CODE 14	CLASS 01	DWG NO. 162072	REV A
ISSUED	SCALE NONE			SHEET 5	

9300023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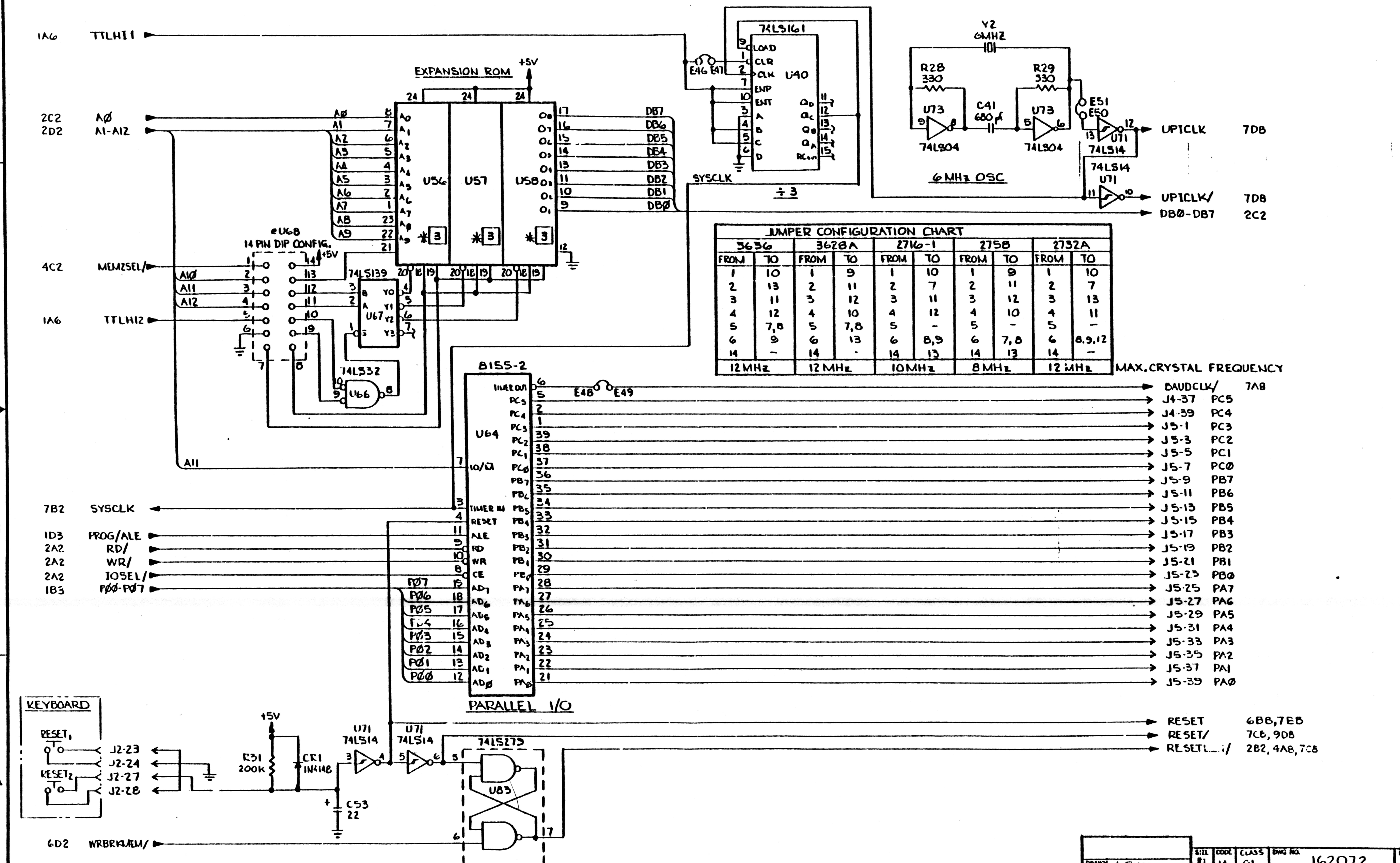
DWG NO. 162072
SH 4
REV A
REVISIONS
ZONE REV DESCRIPTION DFT CHK DATE APPROVED
SEE SHEET 1
2D2 A13
2D2 A14
2D2 A15
2C2 DB0-DB7
1A6 TTLHI1
2C2 AØ
2D2 A1-A12
3B1 RAMWR/
2B2 MONHISEL/
2A2 MONLOSEL/
5A2 RESETLCH/
74LS139
U67
74LS138
U51
74LS32
U72
MEMHISEL/
+5V
RP4 2.2K
W20
W24
W28
W32
W21
W25
W29
W33
W22
W26
W30
W34
W23
W27
W31
W35
BRKPTSEL/ 6C8
MEM2SEL/ 5C8
MEMØSEL/ 3C8
ADDRESS RANGE
0000/1FFF
2000/3FFF
4000/5FFF
6000/7FFF
U30 2114A-5 TYP 16 PLACES
U31 U32 U33 U34 U35 U36 U37
U43 U44 U45 U46 U47 U48 U49 U50
DBØ DB1 DB2 DB3 DB4 DB5 DB6 DB7
WR
MEMORY ONE
2732A
U59 EØØØH
U60 FØØØH
MONITOR ROM
74LS08
U52
74LS04
U73
DRAWN J.CHERRAL
ISSUED
SIZE D
CODE 14
CLASS 01
DWG NO. 162072
REV A
SCALE NONE
SHEET 2
9300023

DWG NO. 162072 SH 5 REV A

REVISIONS: SEE SHEET 1



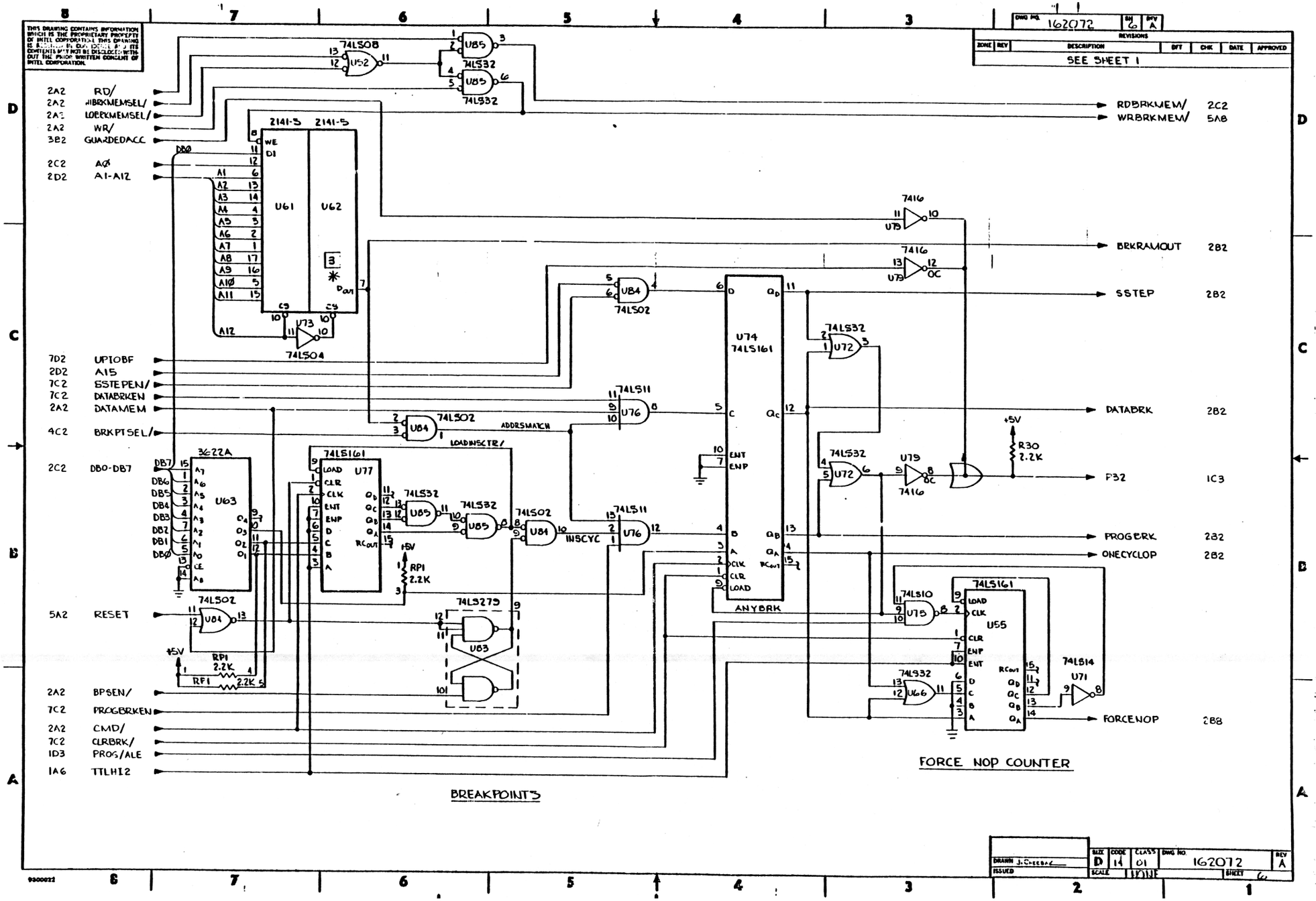
1A6 TTLHI1
EXPANSION ROM
+5V
2C2 AØ
2D2 A1-A12
U56
U57
U58
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DBØ
74LS161
U40
E46 E47
SYSCLK
÷ 3
Y2
6MHZ
R28
330
R29
330
C41
680
U73
74LS04
E51
E50
U71
74LS14
UPICLK 7D8
UPICLK/ 7D8
DBØ-DB7 2C2
6MHz OSC
4C2 MEM2SEL/
1A6 TTLHI2
A1Ø
A11
A12
U68
14 PIN DIP CONFIG.
74LS139
U67
74LS32
U66
8155-2
U64
E48 E49
BAUDCLK/ 7A8
J4-37 PC5
J4-39 PC4
J5-1 PC3
J5-3 PC2
J5-5 PC1
J5-7 PCØ
J5-9 PB7
J5-11 PB6
J5-13 PB5
J5-15 PB4
J5-17 PB3
J5-19 PB2
J5-21 PB1
J5-23 PBØ
J5-25 PA7
J5-27 PA6
J5-29 PA5
J5-31 PA4
J5-33 PA3
J5-35 PA2
J5-37 PA1
J5-39 PAØ
7B2 SYSCLK
1D3 PROG/ALE
2A2 RD/
2A2 WR/
2A2 IOSEL/
1B3 PØØ-PØ7
PARALLEL I/O
KEYBOARD
RESET1
RESET2
J2-23
J2-24
J2-27
J2-28
+5V
R31
200K
CR1
IN4148
C53
22
74LS279
U83
RESET 6B8, 7E8
RESET/ 7C8, 9D8
6D2 WRBRKVEM/

JUMPER CONFIGURATION CHART										
	3636		3628A		2716-1		2758		2732A	
	FROM	TO	FROM	TO	FROM	TO	FROM	TO	FROM	TO
	1	10	1	9	1	10	1	9	1	10
	2	13	2	11	2	7	2	11	2	7
	3	11	3	12	3	11	3	12	3	13
	4	12	4	10	4	12	4	10	4	11
	5	7,8	5	7,8	5	–	5	–	5	–
	6	9	6	13	6	8,9	6	7,8	6	8,9,12
	14	–	14	·	14	13	14	13	14	–
MAX. CRYSTAL FREQUENCY	12 MHz		12 MHz		10 MHz		8 MHz		12 MHz	

DRAWN J. CREBAK — ISSUED

SIZE D | CODE 14 | CLASS 01 | DWG NO. 162072 | REV A

SCALE NONE | SHEET 5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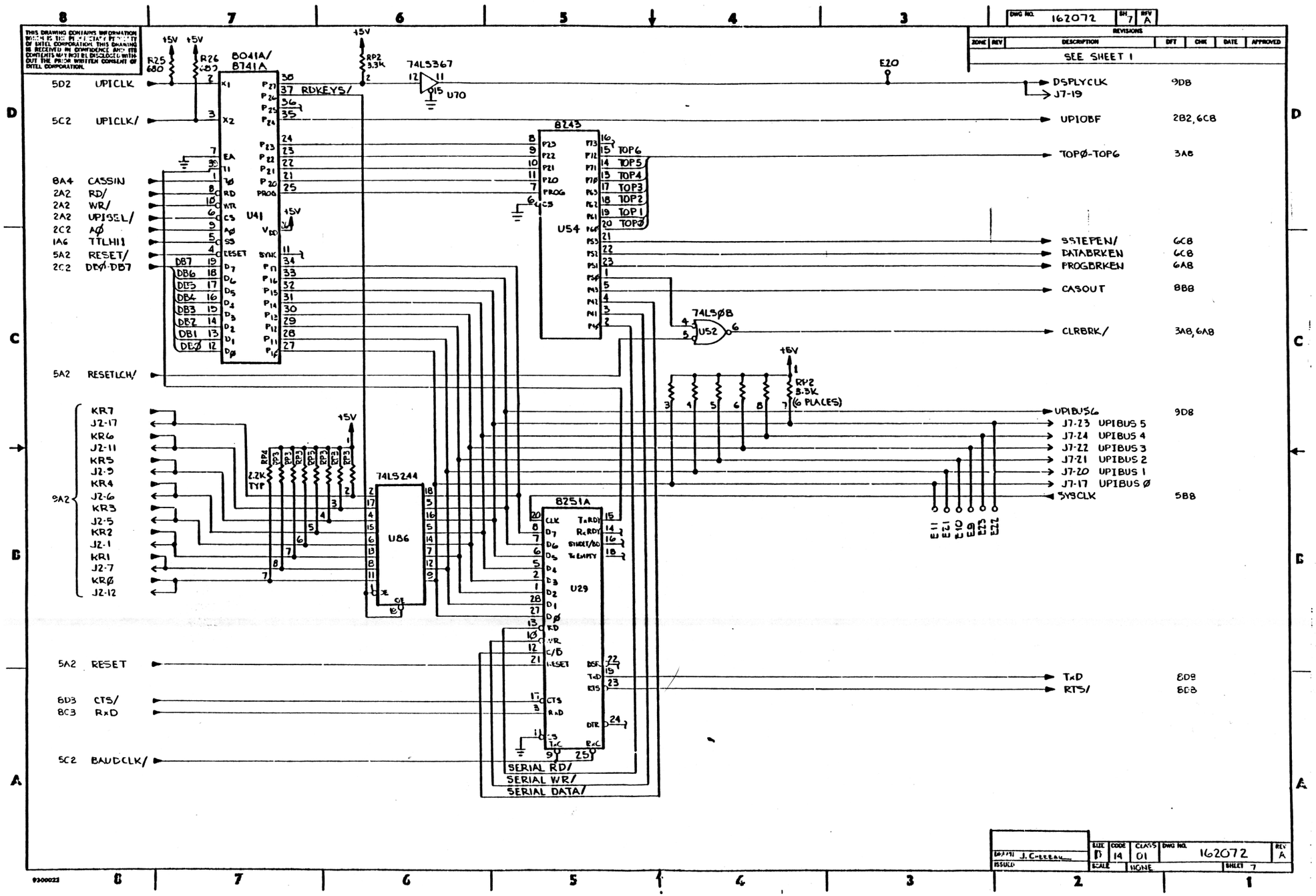
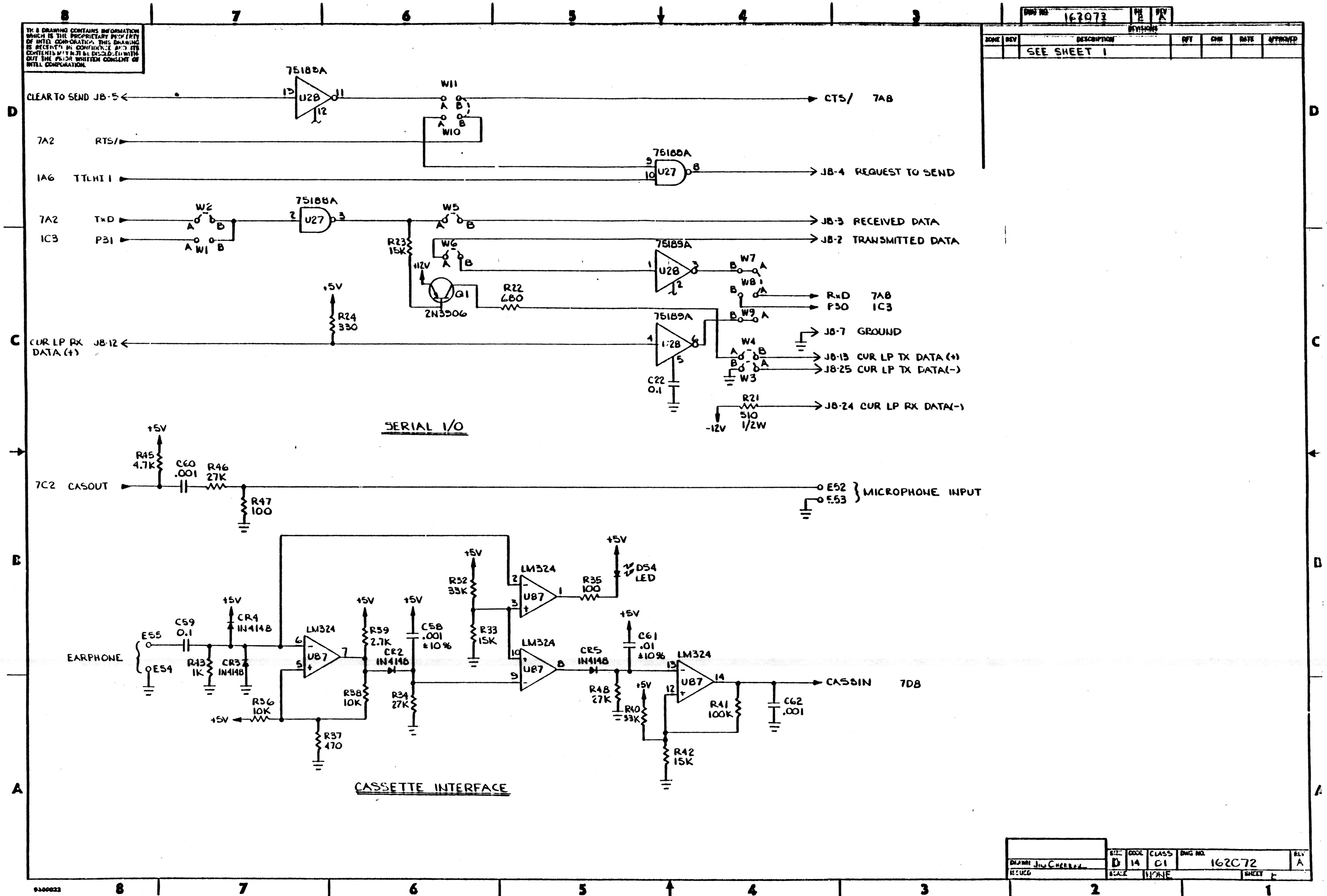
DWG NO. 162072
REVISIONS
ZONE | REV | DESCRIPTION | DFT | CHK | DATE | APPROVED
SEE SHEET 1
2A2 RD/
2A2 MIBRKMEMSEL/
2A2 LOBRKMEMSEL/
2A2 WR/
3B2 GUARDEDACC
2C2 A0
2D2 A1-A12
7D2 UPIOBF
2D2 A15
7C2 SSTEPEN/
7C2 DATABRKEN
2A2 DATAMEM
4C2 BRKPTSEL/
2C2 DB0-DB7
5A2 RESET
2A2 BPSEN/
7C2 PROGBRKEN
2A2 CMD/
7C2 CLRBRK/
1D3 PROG/ALE
1A6 TTLHI2
RDBRKVIEW/ 2C2
WRBRKMEM/ 5A8
BRKRAMOUT 2B2
SSTEP 2B2
DATABRK 2B2
P32 1C3
PROGBRK 2B2
ONECYCLOP 2B2
FORCENOP 2B8
74LS08 U52
74LS32 U85
74LS32 U85
2141-5 U61
2141-5 U62
74LS04 U73
74LS02 U84
74LS11 U76
74LS02 U84
ADDRSMATCH
LOADINSCTR/
74LS161 U77
3622A U63
74LS32 U85
74LS32 U85
74LS02 U81
INSCYC
74LS11 U76
74LS32 U85
74LS279 U83
RP1 2.2K
RF1 2.2K
74LS02 U84
74LS161 U74
ENT
ENP
CLK
CLR
LOAD
ANYBRK
7416 U75
7416 U79 OC
74LS32 U72
74LS32 U72
U79 7416 OC
+5V
R30 2.2K
74LS10 U75
74LS161 U55
74LS32 U66
74LS14 U71
FORCE NOP COUNTER
BREAKPOINTS
DRAWN J.CHEEBAK
ISSUED
SIZE D | CODE 14 | CLASS 01 | DWG NO 162072 | REV A
SCALE NONE | SHEET 6
9300022


8041A/
8741A
U41
74LS367
U70
8243
U54
74LS08
U52
74LS244
U86
8251A
U29
RP2
3.3K
RP1
2.2K TYP
RP2
3.3K
(6 PLACES)
SEE SHEET 1
DSPLYCLK
J7-19
UPIOBF
TOP0-TOP6
SSTEPEN/
DATABRKEN
PROGBRKEN
CASOUT
CLRBRK/
UPIBUS6
J7-23 UPIBUS 5
J7-24 UPIBUS 4
J7-22 UPIBUS 3
J7-21 UPIBUS 2
J7-20 UPIBUS 1
J7-17 UPIBUS 0
SYSCLK
TxD
RTS/
UPICLK
UPICLK/
RESET/
RESETLCH/
RESET
CTS/
RxD
BAUDCLK/
SERIAL RD/
SERIAL WR/
SERIAL DATA/
KR7
KR6
KR5
KR4
KR3
KR2
KR1
KR0
CASSIN
RD/
WR/
UPISEL/
TTLHI1
DB0-DB7
RDKEYS/
TOP6
TOP5
TOP4
TOP3
TOP2
TOP1
TOP0
E20
E11
E12
E10
E9
E13
E22



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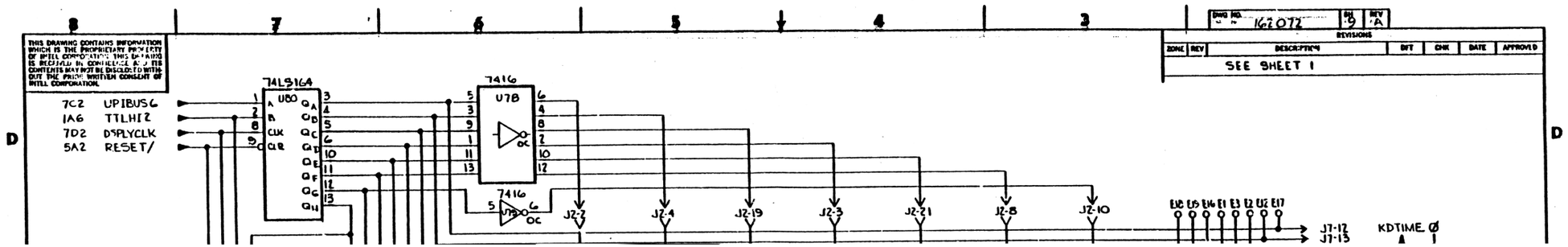
DWG NO. 162073 REV A
REVISIONS
ZONE REV DESCRIPTION DFT CHK DATE APPROVED
SEE SHEET 1
CLEAR TO SEND J8-5
75188A
U28
W11
W10
CTS/ 7A8
7A2 RTS/
1A6 TTLHI 1
75188A
U27
J8-4 REQUEST TO SEND
7A2 TxD
1C3 P31
W2
W1
U27
W5
J8-3 RECEIVED DATA
W6
J8-2 TRANSMITTED DATA
R23 15K
+12V
Q1
2N3906
R22 680
75189A
U28
W7
W8
RxD 7A8
P30 1C3
W9
+5V
R24 330
75189A
U28
J8-7 GROUND
CUR LP RX DATA (+) J8-12
W4
W3
J8-13 CUR LP TX DATA (+)
J8-25 CUR LP TX DATA(−)
C22 0.1
R21 510 1/2W
-12V
J8-24 CUR LP RX DATA(−)
SERIAL I/O
+5V
R45 4.7K
C60 .001
R46 27K
7C2 CASOUT
R47 100
E52
E53
MICROPHONE INPUT
+5V
LM324
U87
R35 100
D54 LED
R32 33K
R33 15K
EARPHONE
E55
E54
C59 0.1
R43 1K
CR3 1N4148
CR4 1N4148
LM324
U87
R39 2.7K
CR2 1N4148
C58 .001 ±10%
R36 10K
R38 10K
R34 27K
R37 470
LM324
U87
CR5 1N4148
C61 .01 ±10%
R48 27K
R40 33K
LM324
U87
R41 100K
R42 15K
C62 .001
CASSIN 7D8
CASSETTE INTERFACE
SIZE D CODE 14 CLASS C1 DWG NO. 162C72 REV A
DRAWN Jim Cherry
SCALE NONE SHEET 8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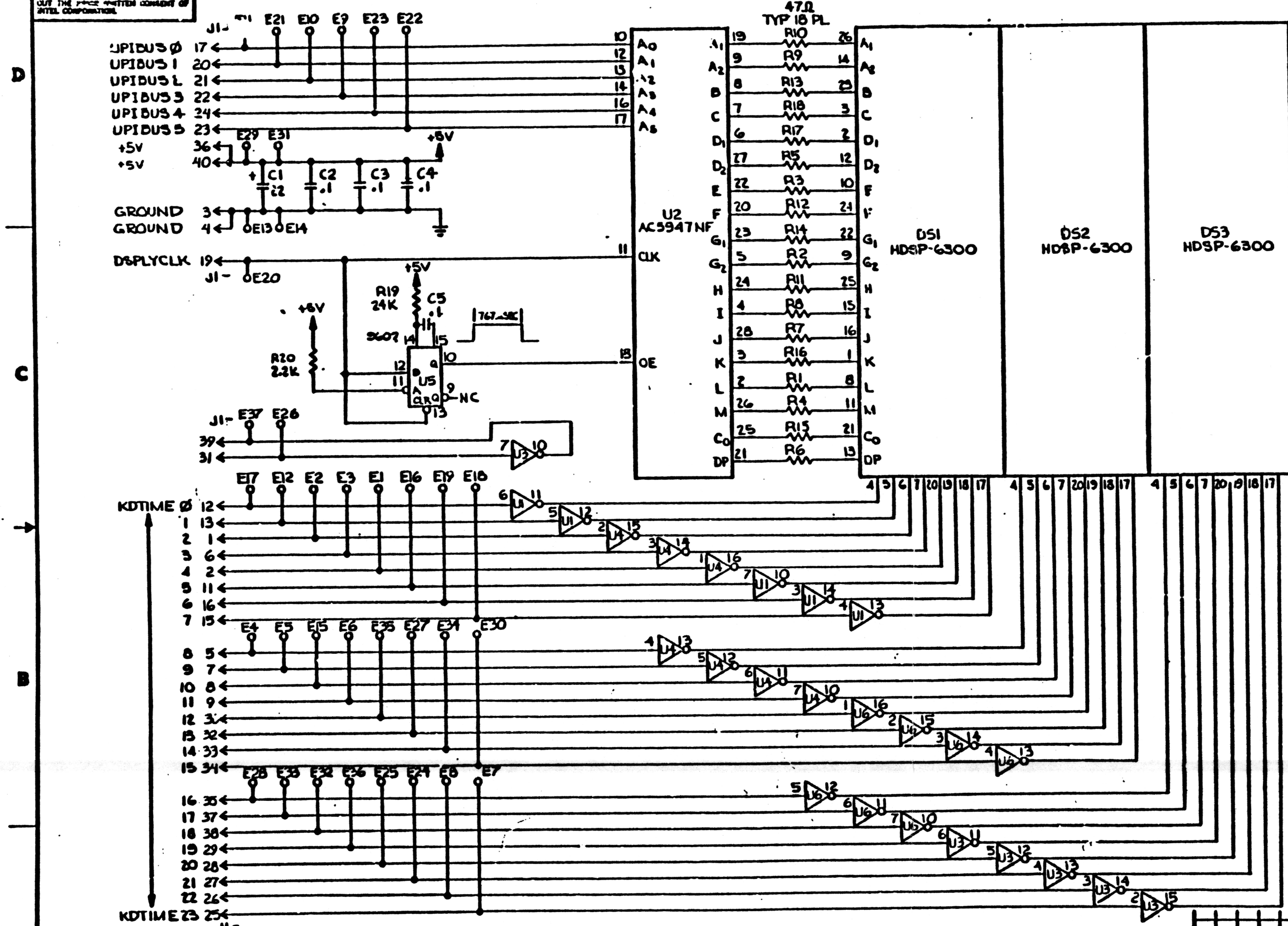
DWG NO. 162072
SH 9
REV A
REVISIONS
ZONE REV DESCRIPTION DFT CHK DATE APPROVED
SEE SHEET 1
7C2 UPIBUS6
1A6 TTLHIZ
7D2 DSPLYCLK
5A2 RESET/
74LS164
U80
74S16
U78
74S16
U79
J2-7
J2-4
J2-19
J2-3
J2-21
J2-5
J2-10
E16 E15 E14 E1 E3 E2 E12 E17
J7-17
J7-15
KDTIME Ø
J7-11



DWG NO.	SH	REV
162075	1	B

REVISIONS

ZONE	REV	DESCRIPTION	DFT	CHK	DATE	APPROVED
	A	ECO 14-0250	11-3-80		11-17-80	
	B	ECO 14-0277			1-6-81	

POWER AND GROUND LOCATOR CHART			
REF DESIG	DEVICE TYPE	+5V	GND
U2	AC5947NF	1	15
U5	9602	16	8
U1,3,4,6	ULN2003A	9	8
DS1 - DS3	HDSP-6300	-	-

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTANCE VALUES ARE IN OHMS, 1/4W, ±5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL IC DEVICES ARE ULN2003A.
4. THE FOLLOWING TABLE DESCRIBES THOSE PLATED-THRU HOLES THAT HAVE 1) AN 'E' REF DESIGNATOR AND 2) A PIN NUMBER FOR CONNECTOR J1.

E	J1
13	4
15	8
17	12
19	16
21	20
23	24
25	28
27	32
29	36
31	40

USED ON ASSY No
162315
162073

SPARES

TYPE	REF DESIG	QTY
ULN2003A	U3	1
9602	U5	1
ULN2003A	U1	2

REF DESIGNATION

LAST USED	NOT USED
DS3	
U6	
R20	
J1	
E37	
C5	

NEXT ASSY	USED ON
162315	SDK-2920
162073	SDA-51

UNLESS OTHERWISE SPECIFIED

SIGNATURE	DATE
DRN BY Jim Coleman	3-3-80
CHK BY	
ENGR APVD	
APVD	
APVD	

intel
3065 BOWERS AVE.
SANTA CLARA
CALIF. 95051

TITLE: SCHEMATIC, DISPLAY

SIZE	CODE	CLASS	DWG NO.	REV
D	14	01	162075	B

SCALE: NONE
SHEET 1 OF 1